SYNOPSYS®

SUCCESS STORY

Synopsys & Amazon Web Services

Leveraging Existing High Speed Functional Serial Interfaces for Testing & Monitoring

"Synopsys SLM High-Speed Access & Test IP allowed us to conduct scan test over a functional interface. This enabled running scan test through the entire silicon lifecycle including—Wafer Sort, Final Test, System-Level Test, and In-System Test."

~Amit Pandey, Principal Engineer ASIC at AWS

aws

Project Overview

High-speed functional interfaces such as PCIe and USB can perform double duty as high-speed test access interfaces addressing multiple design challenges. Synopsys has collaborated closely with Amazon Web Services (AWS) over the last few years to create and implement a unique solution that leverages an existing functional protocol-based high speed interface for testing and monitoring which has provided a consistent portable method to test silicon throughout its lifecycle.

Challenges

Advanced node and larger chip designs experience numerous challenges in order to achieve reliable silicon operation over their entire lifecycle. Modern SoC's are implemented in many mission-critical applications which require a very low defective-parts-per-million (DPPM) metric. There are two ways to guarantee low DPPM - continuous testing and monitoring of semiconductor devices throughout their lifecycle and increased test coverage. At the same time there is pressure to reduce the number of pins on the SoC, making it difficult to meet test time and cost goals.

Traditional pins used for scan testing operate in the frequency range of 50Mhz—200Mhz. Until a few generations ago, such speeds were enough to fully utilize the test bandwidth as designs consumed test data at a much lower rate compared to what the pins could deliver. Today's designs have grown significantly in their size and the rate at which they can consume scan data has increased exponentially. Now, the operating speed of the scan pins is a limiting factor in today's designs and driving the scan networks via high-speed interfaces is a necessity to provide higher test bandwidth to the SoC. The increase in the number of scan chains results in more test pins being needed in today's SoC's. HSAT IP leverages the existing pins of the functional interface alleviating the problem caused by limited General Purpose I/Os (GPIOs). Scan tests provide a valuable mechanism for debugging silicon at any stage and an HSAT-based scan test can be conducted at any stage of the silicon lifecycle.

Synopsys Solution

The Synopsys SLM High-Speed Access and Test (HSAT) IP solution takes advantage of the existing high-speed functional interfaces such as PCIe or USB in the SoC to deliver test data by using the native functional protocol of the interface. High-speed interfaces have been used during functional operation of SoCs for many decades with readily available drivers and hardware and Synopsys SLM HSAT leverages this established infrastructure to deliver scan test data and Test-Access-Port (TAP) data, see Figure 1.

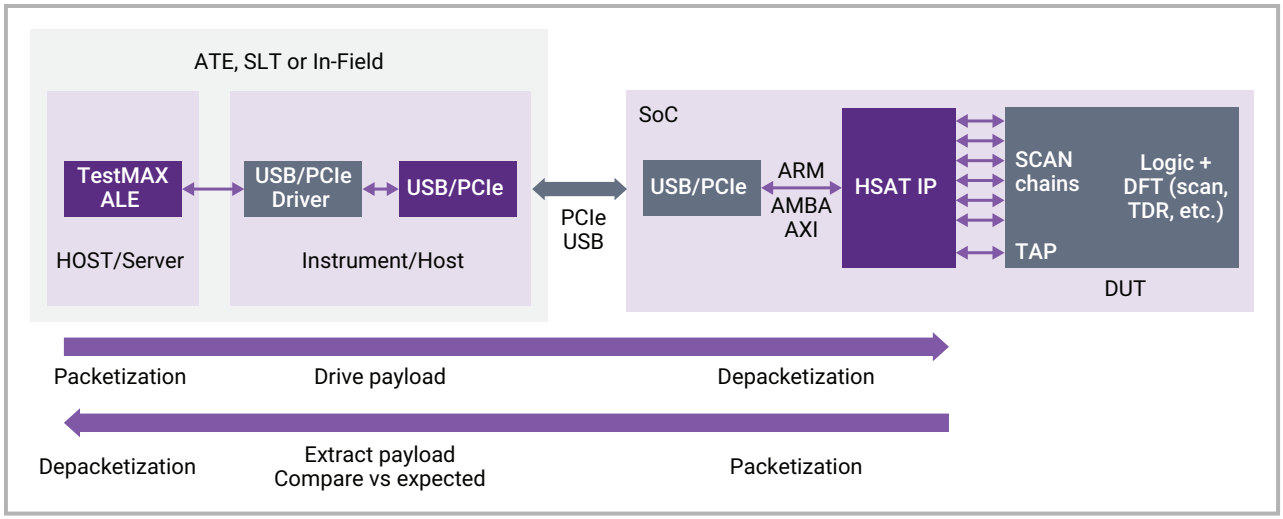

Figure 1: Synopsys SLM HSAT IP solution

Another capability of Synopsys SLM HSAT IP is its ability to leverage the same manufacturing test patterns, functional interfaces, and infrastructure to support System-Level Test (SLT) and In-System Test (IST) without needing access to test pins. The Synopsys SLM HSAT IP solution addresses the bandwidth limitation of GPIO-based interfaces and naturally scales to take advantage of advances in bandwidth of PCIe and USB technology.

Key Benefits of High-Speed Functional Serial Interfaces for Test

- Easily repeat manufacturing tests in-system and in-field
- Reduce test time by eliminating the constraint of GPIO test pin data rate
- Re-use functional HSIO ports (PCIe and USB) for test and monitor data
- Avoid the need for large numbers of GPIO test pins
- Bandwidth scales with each new generation of PCIe/USB

Architecture for AWS ML Server

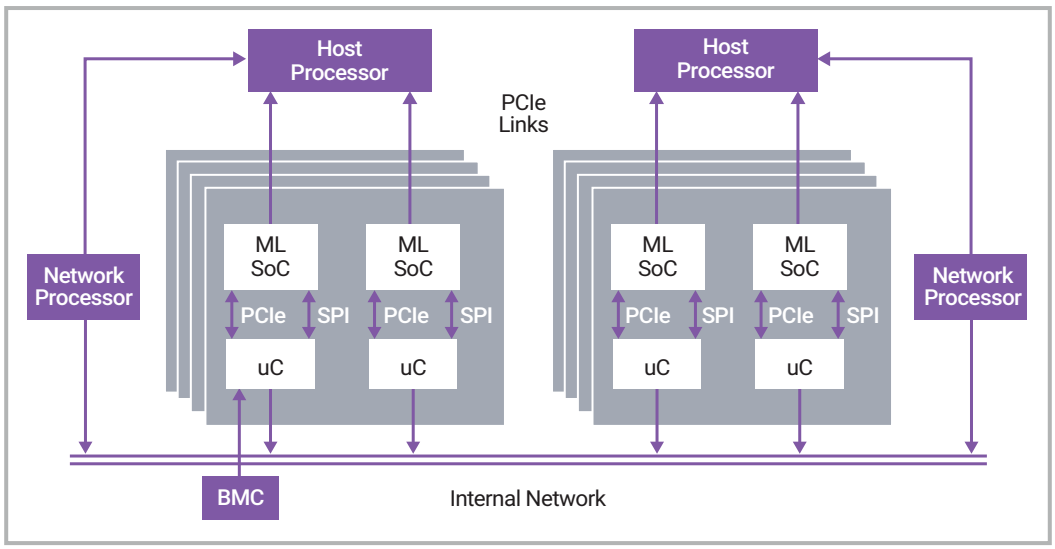

Figure 2: Health monitoring MCU connects to AWS Trainium SoC with Synopsys SLM HSAT

Figure 2 shows the high-level architecture of AWS machine learning (ML) server based on Trainium SoC. Synopsys SLM HSAT IP is integrated into the SoC and can be accessed via an SPI or PCIe interface. Health monitoring MCU's access the SLM HSAT IP on the SoC and run scan test at pre-decided intervals.

Advantages of these architecture are:

- SLM HSAT-based test infrastructure enables SLT , IST and diagnosis of devices throughout their lifecycle
- Root cause analysis of in-field failures due to latent defects or test escape
  - Leverage high quality SCAN vectors without taking device out of the target system
  - Full diagnostic capability of SCAN patterns
- Early indication of degradation or aging type defects
- Augmentation of SCAN pattern for improved fault detection
- Analysis of silent data corruption (SDC) scenarios
- Improve test bandwidth with potential for reduced test time/cost

Expertise and Technical Support Test

Amazon engaged with Synopsys to help address the challenges of data transport in advanced node technologies by using the existing highspeed functional interfaces of an SoC, such as PCIe or USB, to perform both scan test and in-system test with easy accessibility.

"The Synopsys SLM HSAT IP team did an excellent job leveraging Synopsys' internal expertise to provide a novel solution to Amazon which we plan to deploy widely," Amit Pandey, Principal Engineer ASIC at AWS.

Conclusion

Using the functional protocol of an existing high-speed I/O port for testing is a novel approach to solve the problem of reduced GPIO pin availability during manufacturing test. The solution also helps by increasing the bandwidth available for scan testing, thereby reducing test cost and time. Higher bandwidth allows chips to implement a much wider scan network to distribute data to cores, enabling more cores to run in parallel. The frequency of on-chip scan networks can be faster as it is no longer limited by pin timing bottlenecks of regular, slow-speed I/O's. All these factors contribute to higher parallelism and lower cost. The same HSAT-based test infrastructure can be used for enabling in-system test and monitoring throughout the lifecycle of the chip. Synopsys SLM HSAT-based test can also be used to test 3D devices that do not have accessible, low-speed I/Os. High speed access and test IP provides adaptive high bandwidth testing over a functional interface, reducing test time and cost with a lower pin count, enabling testing through entire silicon lifecycle.

For more information about Synopsys SLM HSAT IP, visit the Synopsys website